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MS-7808

ATX

Ver:0A

H/W:Frankyang

PM:Feifei

Intel -MahoBay plamform B75

CPU:

IVY bridge LGA1155

System Chipset:

Panther Point B75

Onboard Chip:

Audio Codec: 887

LAN-RTL8111E colay8105E

SIO:Fintek F71868AD

Flash ROM: SPI 128 MB

Main Memory:

DDRIII (1066/1333/1600MHz) * 2 (Dual Channel)

ACPI:

UPI

PWM:

VRD12 -UT501 3+1 Phase

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 1


PCI Slot * 1

Other: SATA3.0 x1+SATA2.0 x3 (PCH)

USB2.0 *8

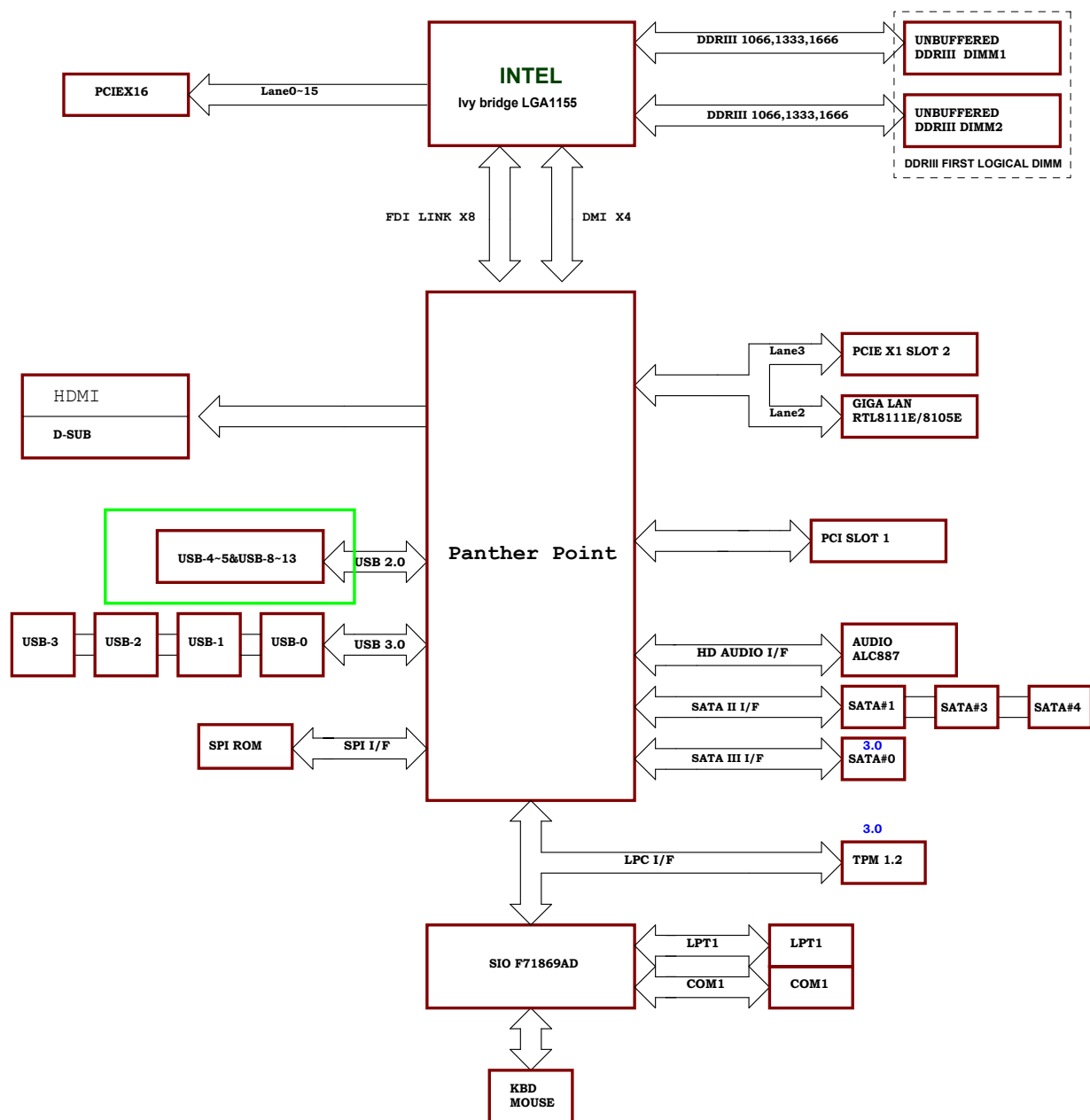
REAL USB3.0 *2

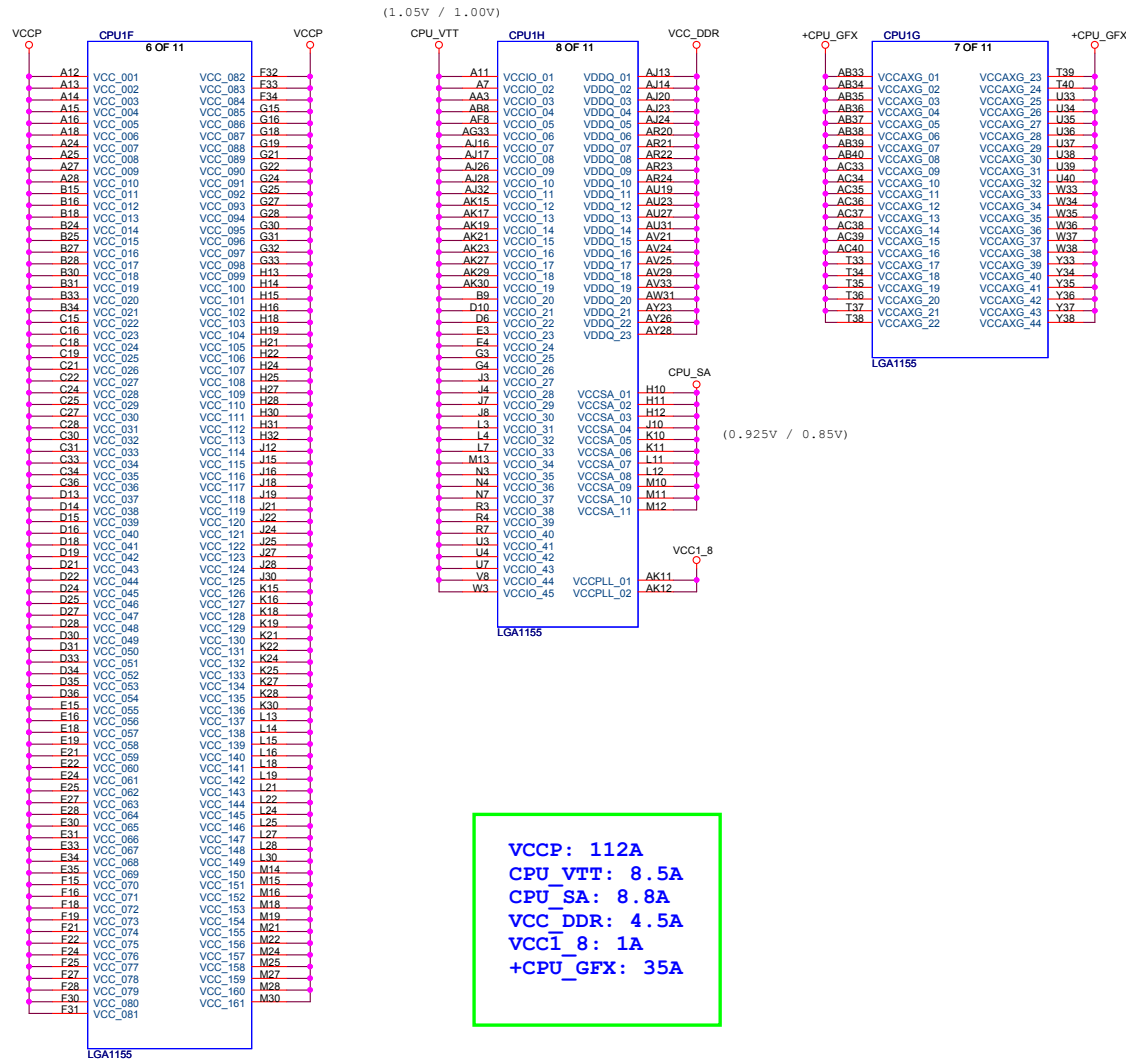
FRONT USB3.0 *2



MICRO-STAR INT'L CO.,LTD		
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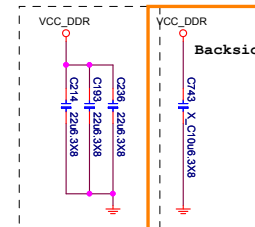
MS-7758 Block Diagram





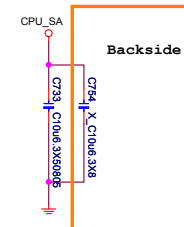
+1.5V_DDR3-Decoupling

CPU SOCKET CAVITY CAPS



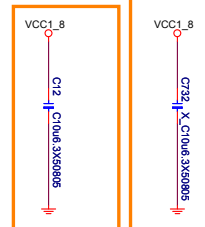
+CPU_SA Decoupling

Backside



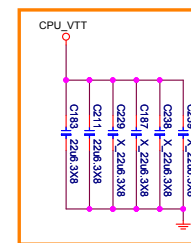
+VCC1_8 Decoupling

Backside

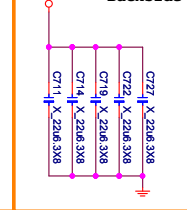


+CPU_VTT Decoupling

CPU SOCKET CAVITY CAPS

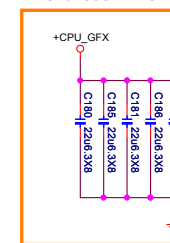


Backside

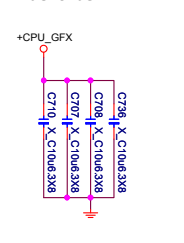


+CPU_GFX Decoupling

CPU SOCKET CAVITY CAPS

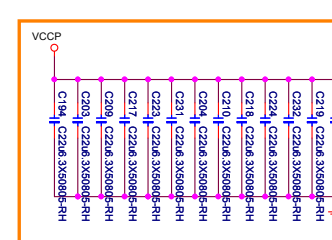


Backside

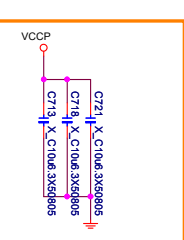


+CPU_VCCP-Decoupling

CPU SOCKET CAVITY CAPS



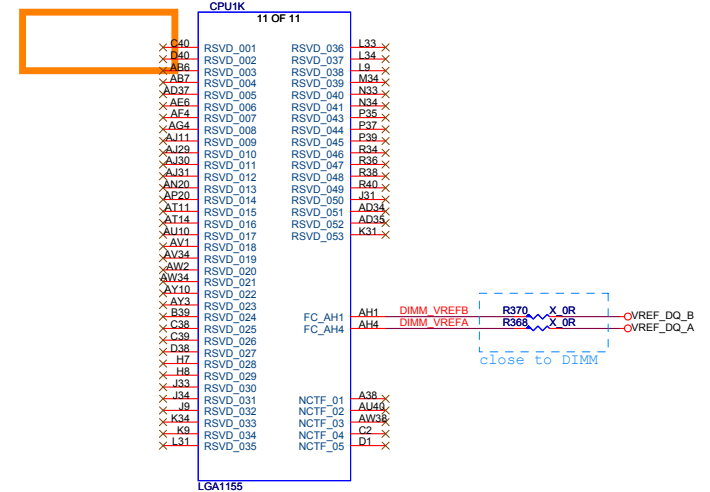
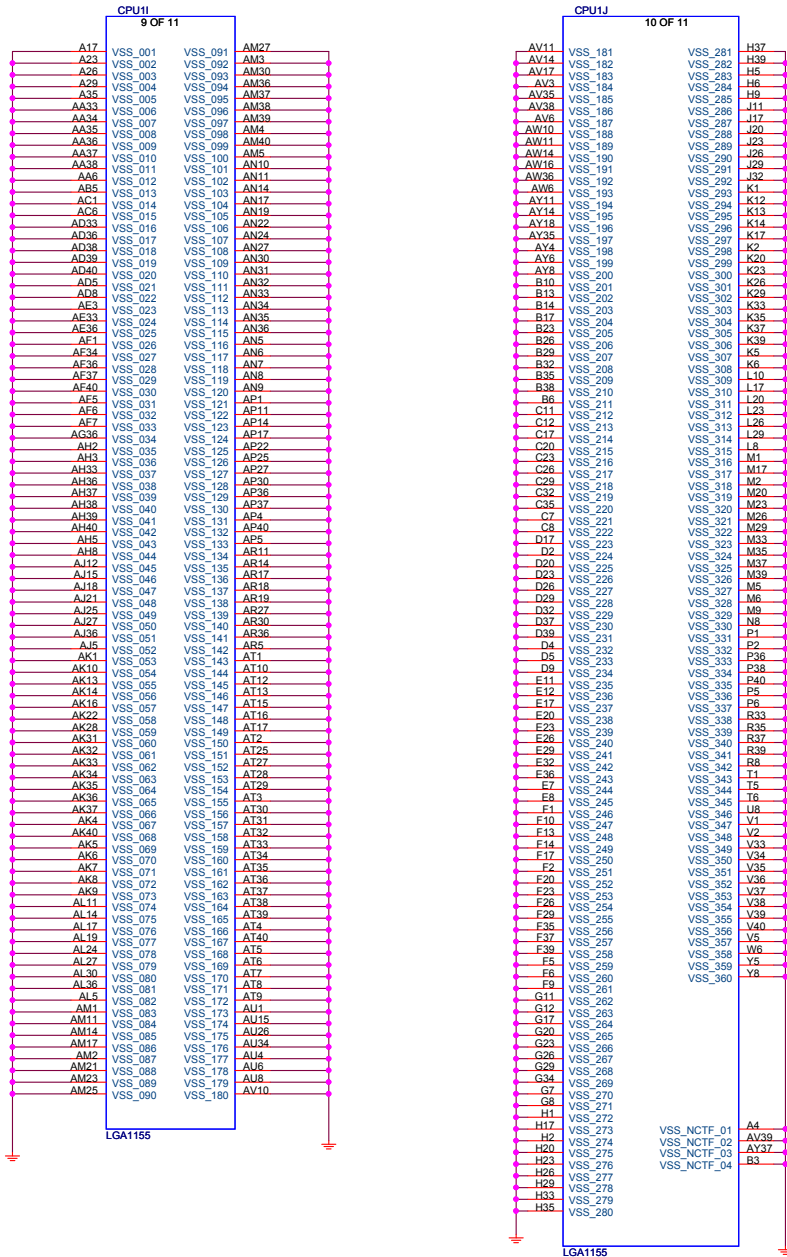
Backside



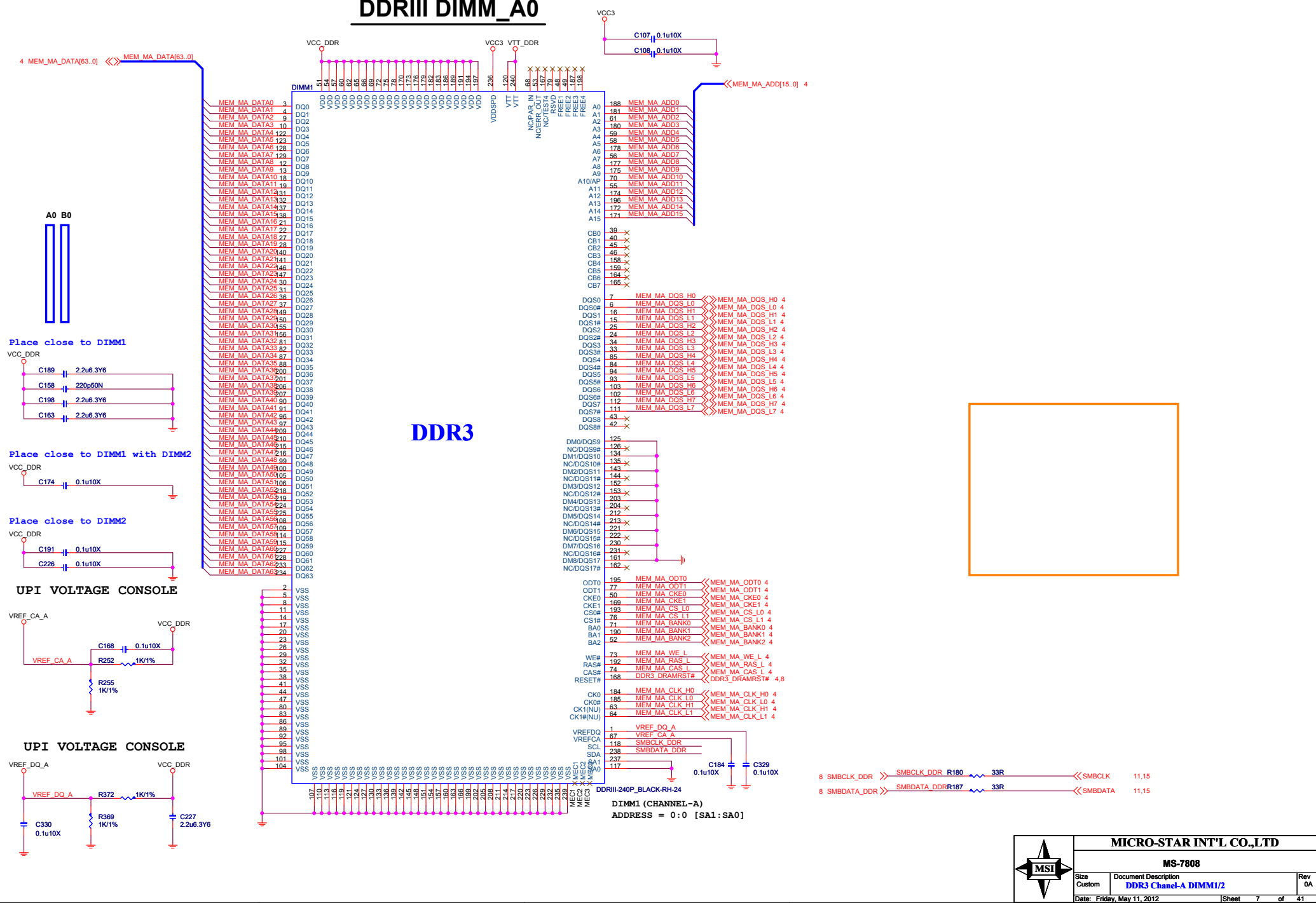
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DDR3 DIMM_A0

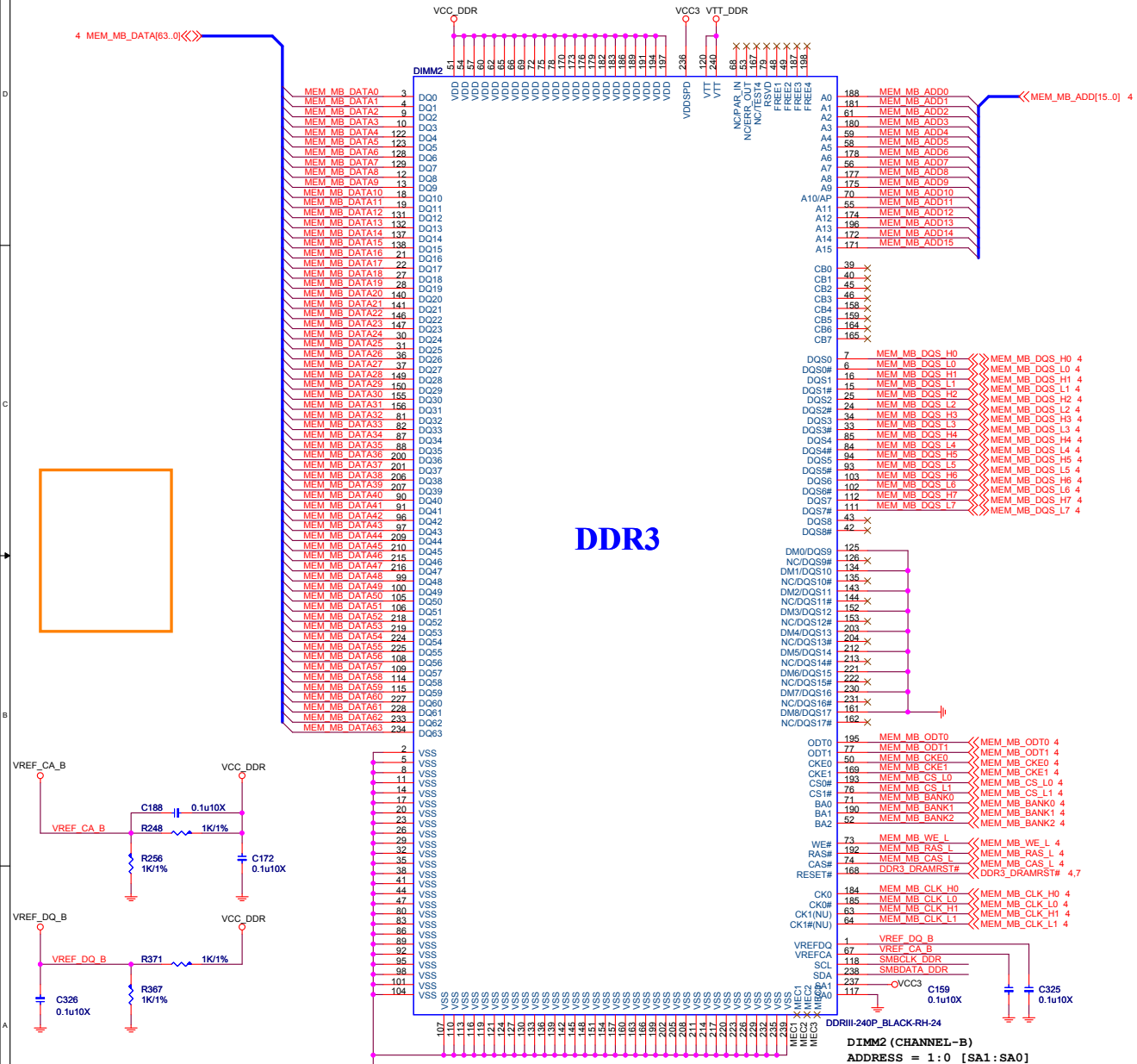


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DDR3 DIMM_B0



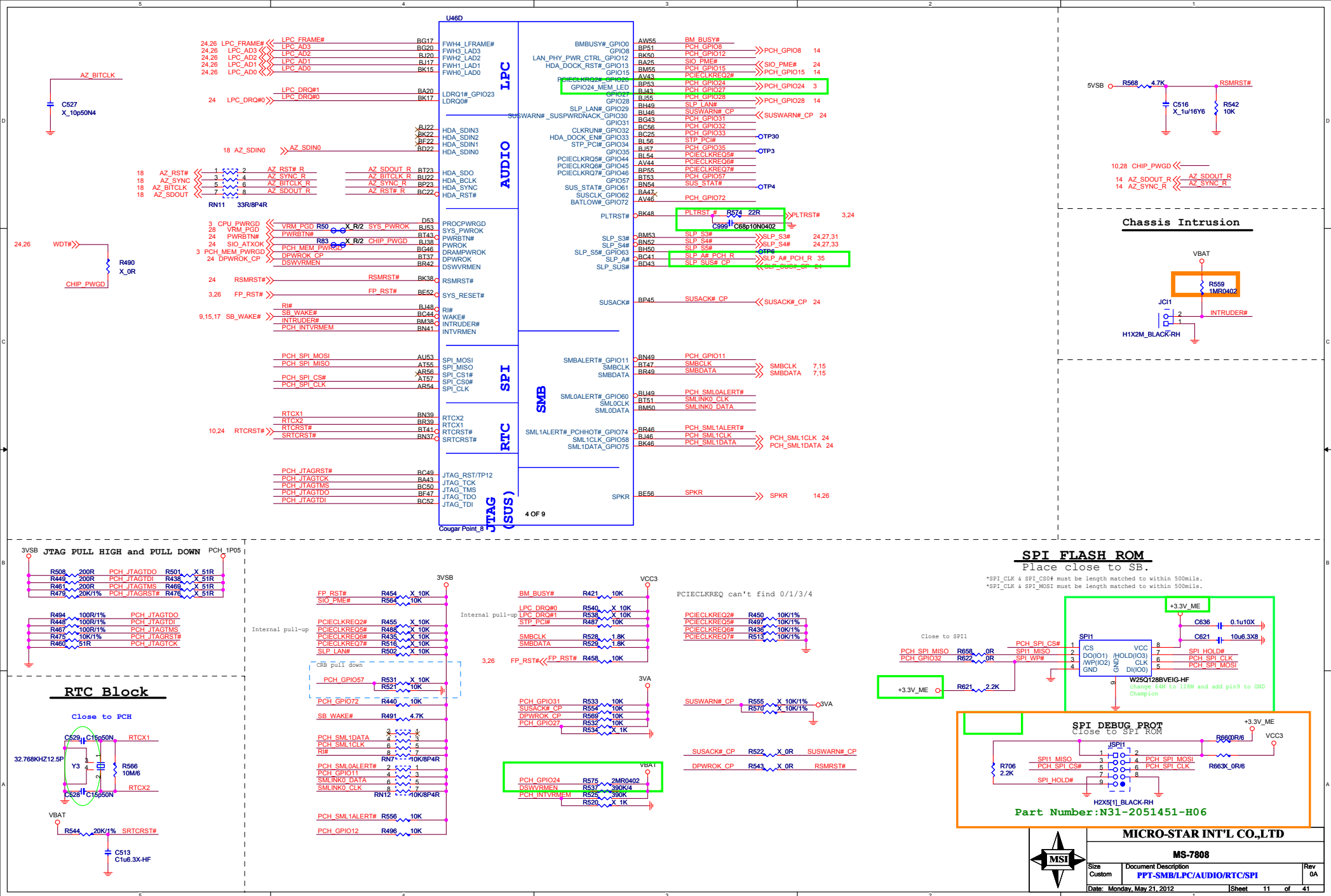
DDR3

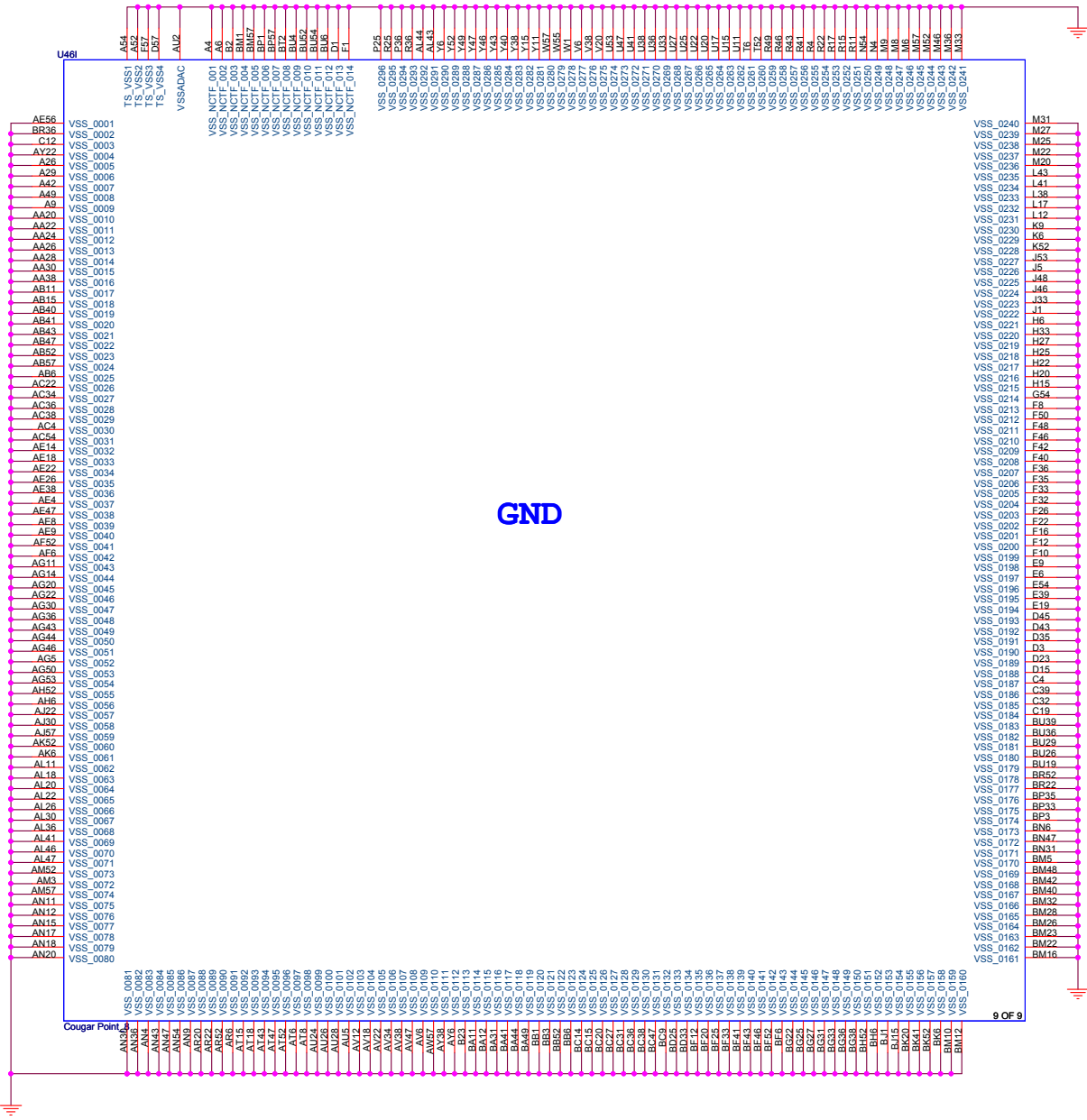
DDR3-240P BLACK-RH-24
DIMM2 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]

SMBCLK_DDR << SMBCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR 7

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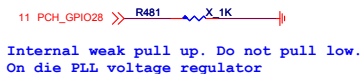
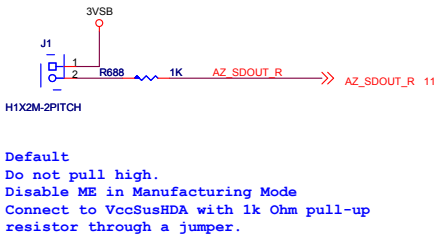
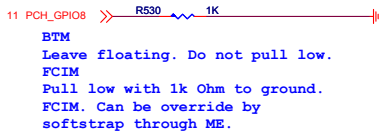
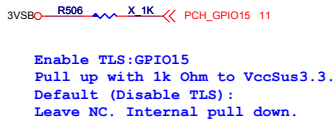
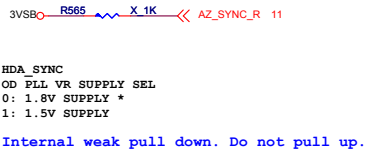
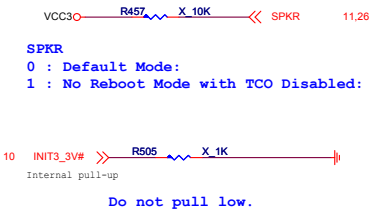






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MS-7808		
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PCH Straps

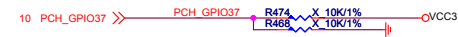


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window

When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.



Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

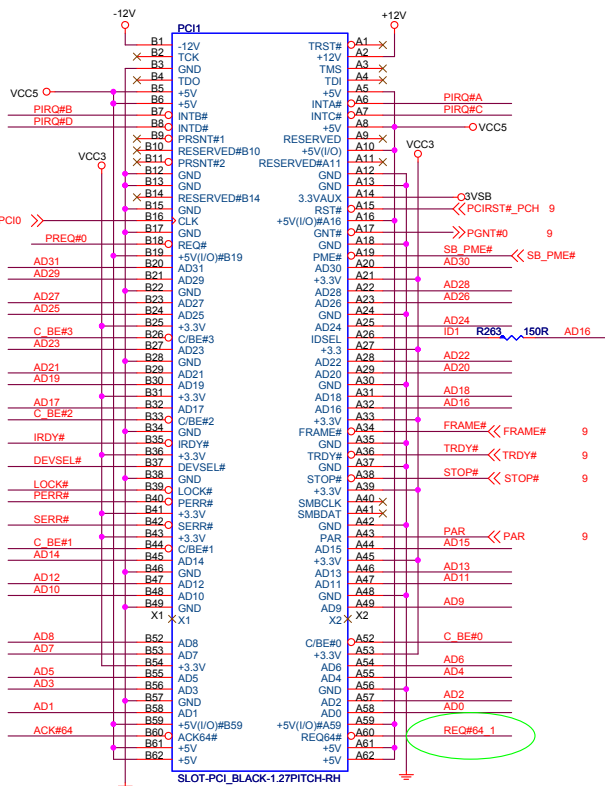
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window

When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.



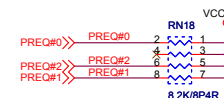
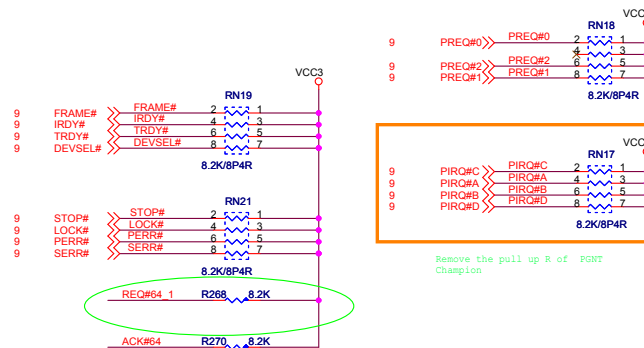
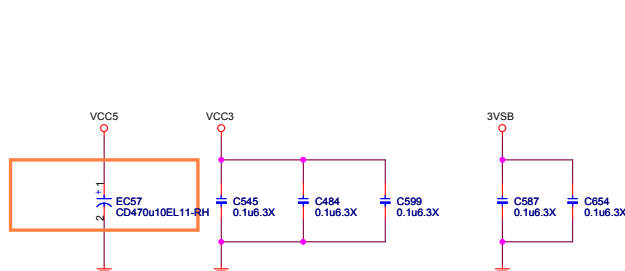
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MS-7808		
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IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

AD[31..0] <<> AD[31..0] 9
 C_BE[3..0] <<> C_BE[3..0] 9

PCI PULL-UP / DOWN RESISTORS



Remove the pull up R of PGT Champion

PCI slot

+3.3Vaux	- 375mA
+3.3V	- 7.6A
+12V	- 0.5A

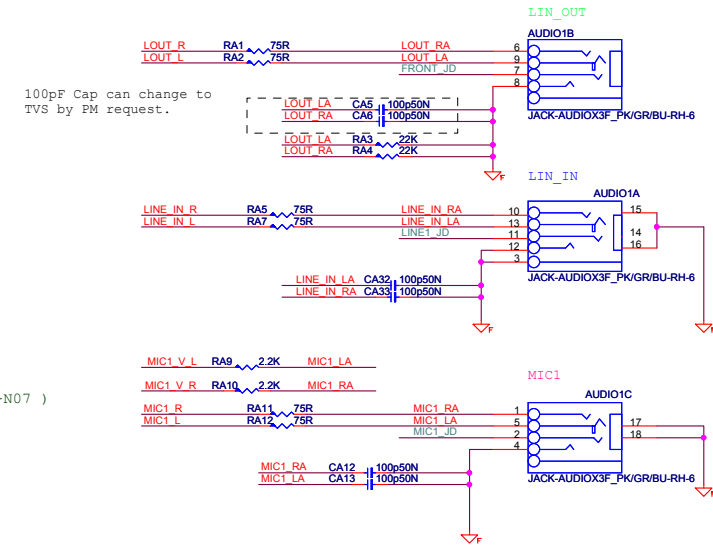
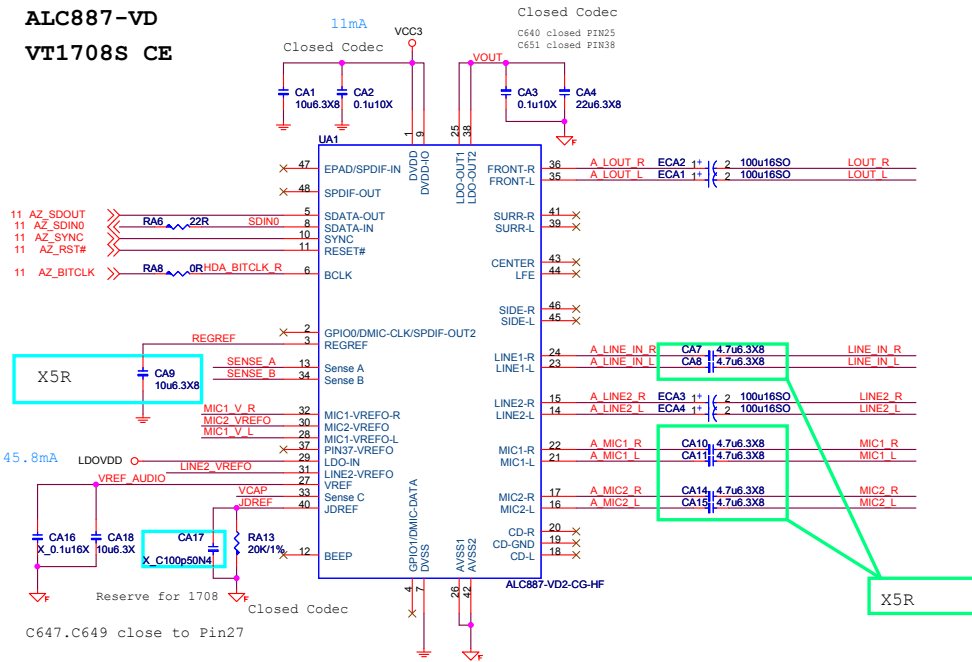


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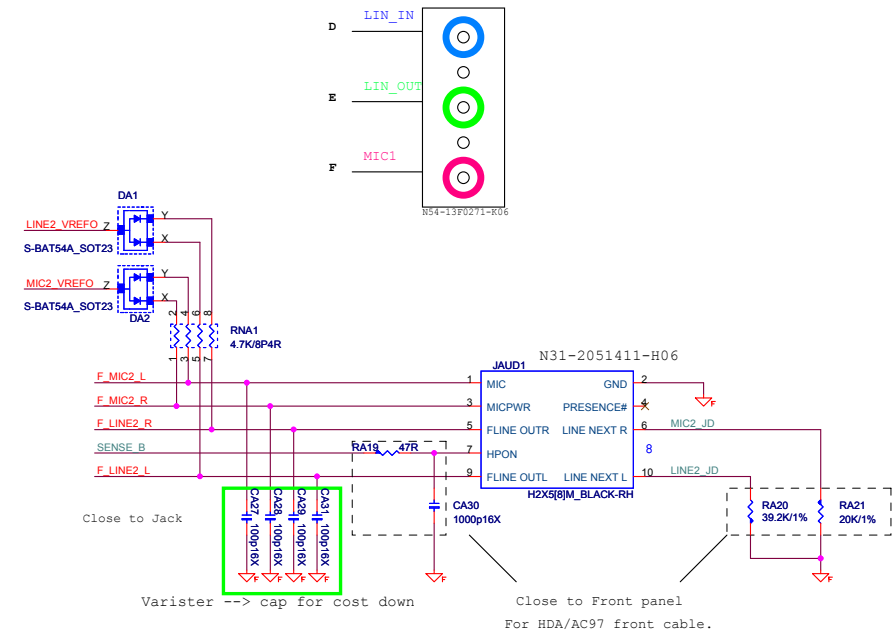
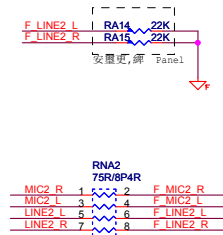
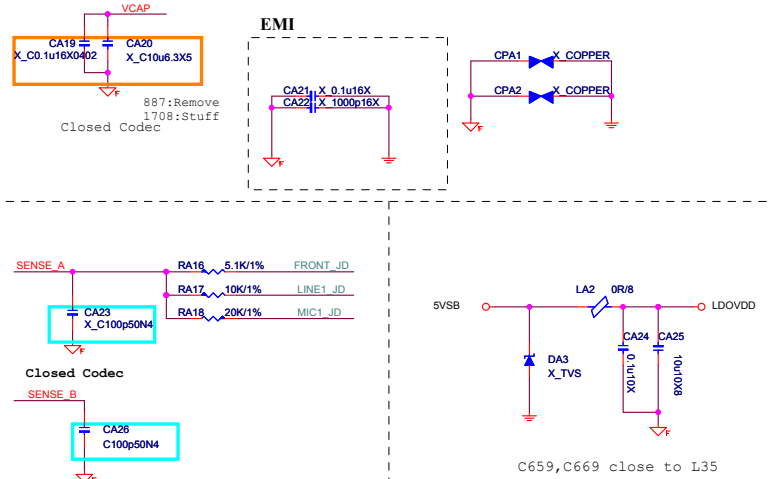
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ALC887-VD
VT1708S CE



EL 100u (C94-1012511-N07)



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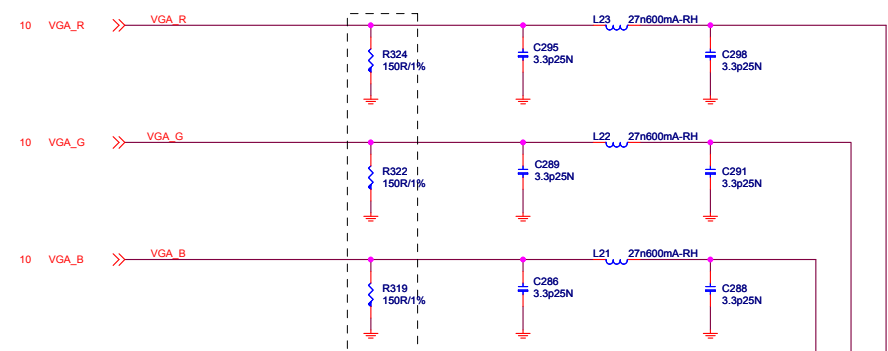
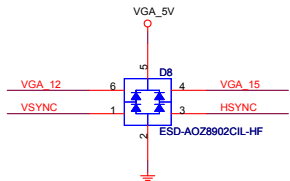
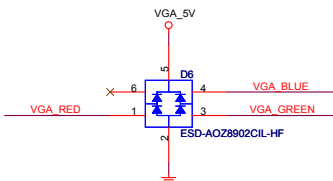
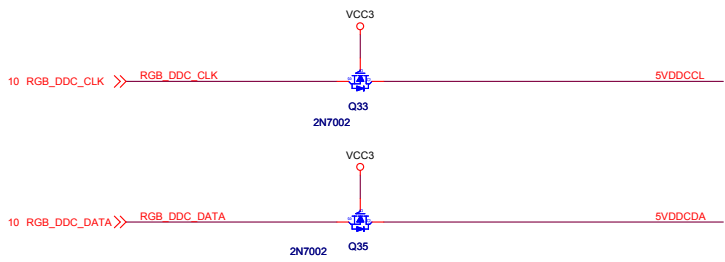
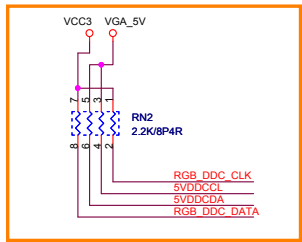
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Size Custom	Document Description Audio Codec ALC887	Rev 0A
Date: Friday, May 11, 2012		Sheet 18 of 41

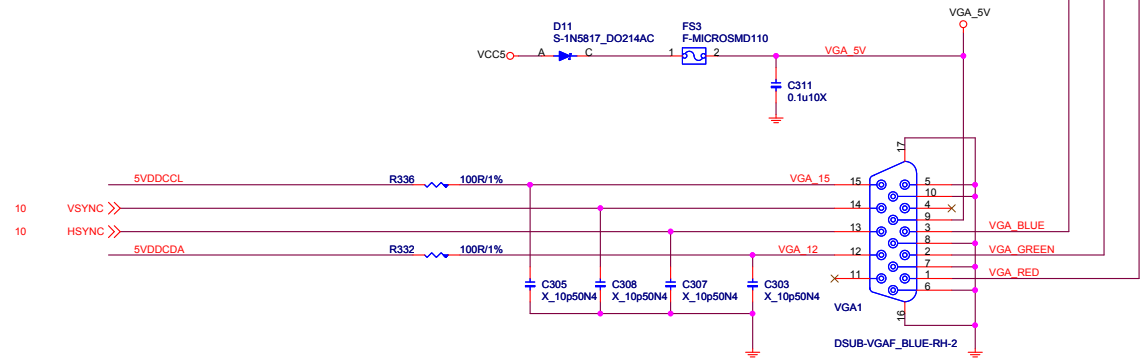
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN

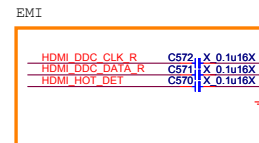
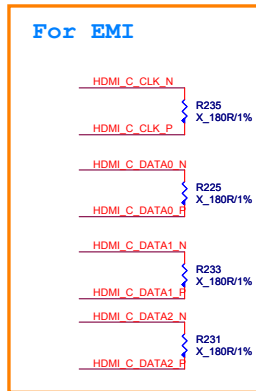
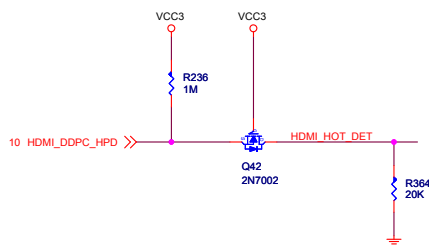
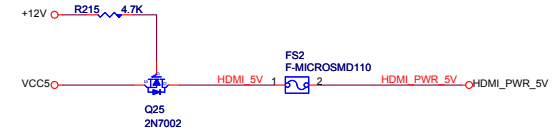
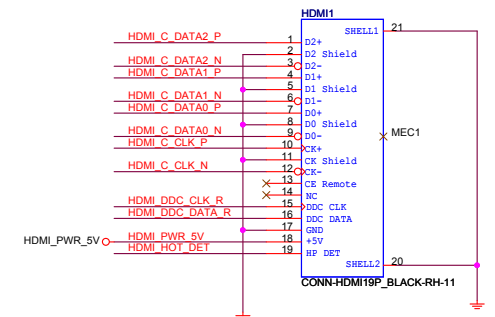
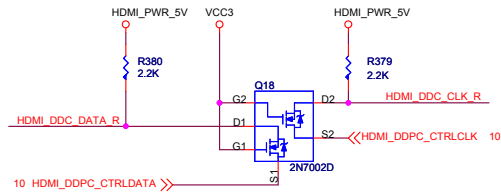
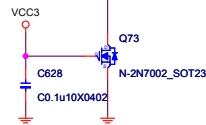
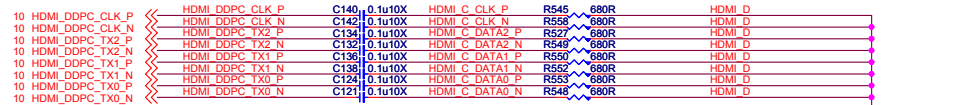


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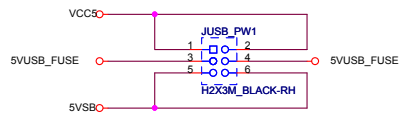
Size	Custom	Document Description	Rev
		VGA Connector	0A
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HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



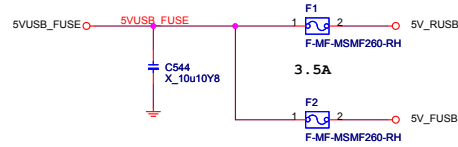
MICRO-STAR INT'L CO.,LTD		
MS-7808		
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5V_RUSB Switch

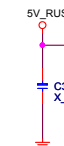
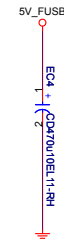
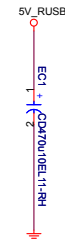


Default VCC5 (PIN1-3,2-4)

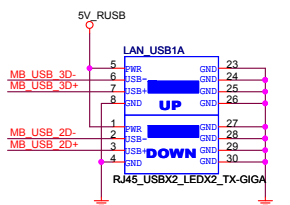
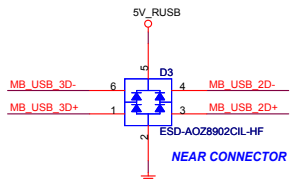
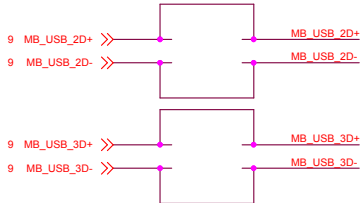
5V_RUSB must 120mm



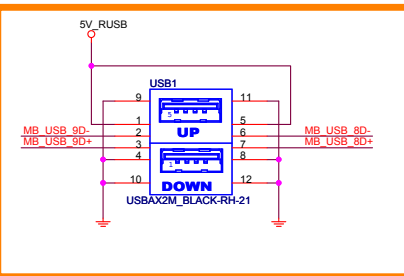
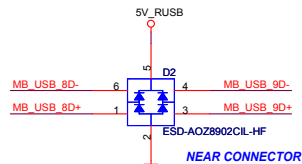
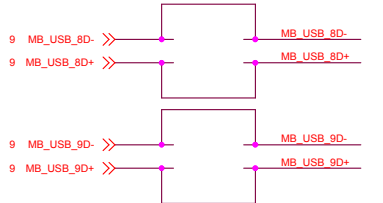
JUSB_FW1	BIOS Menu	Wake up support
1-3,2-4	EUP Enable	Not support
	EUP Disable	Not support
3-5,4-6	EUP Enable	Not support
	EUP Disable	support



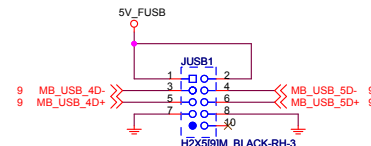
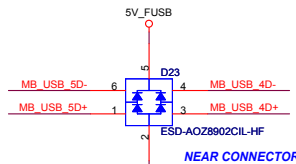
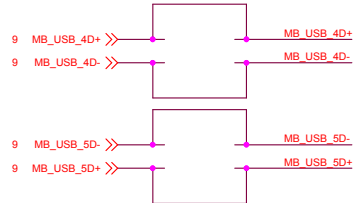
REAR USB PORT 8,9 (With LAN)



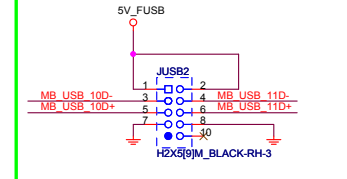
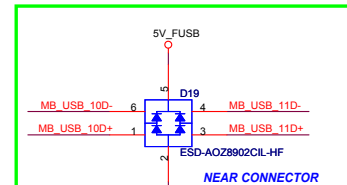
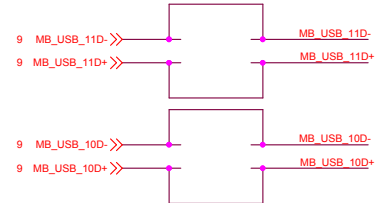
REAR USB PORT 8,9 (USB1)



FRONT USB PORT 0,1



FRONT USB PORT 8,9



Remove USB2.0 PORT 10,11
USB6&USB7
Champion



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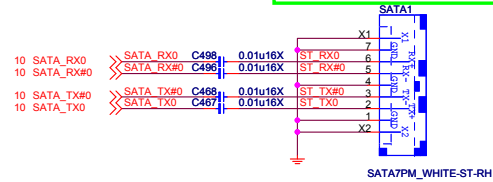
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change SATA5s PORT0,1 to SATA PORT 0

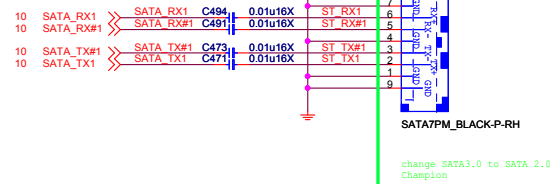
SATA 6G PORT 0

3.0 white

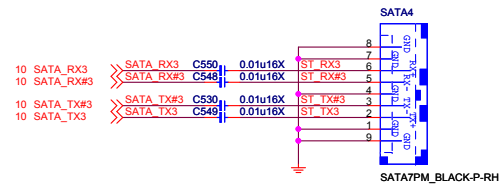
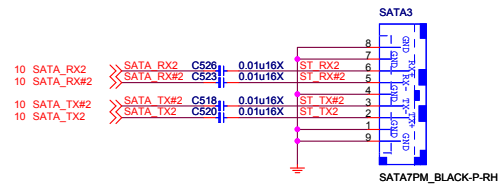


add SATA 3G PORT 1
Champion

SATA 3G PORT 1



SATA 3G PORT 2,3



REMOVE SATA5\6 , Exchange name of sata1 with sata4



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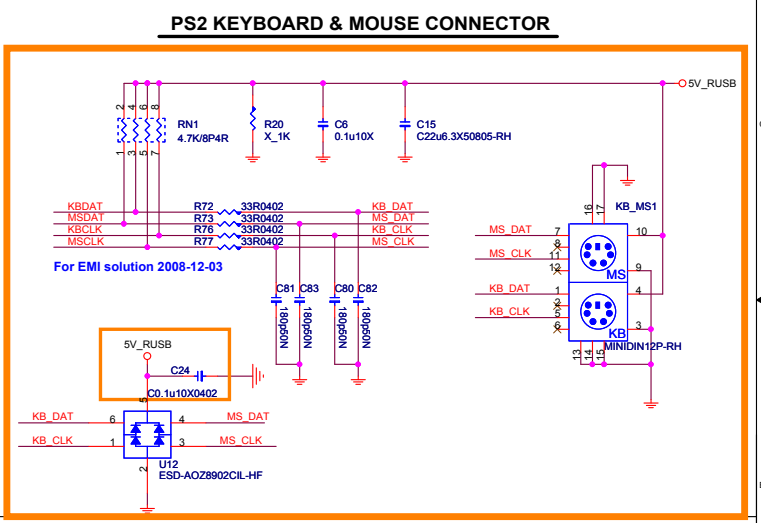
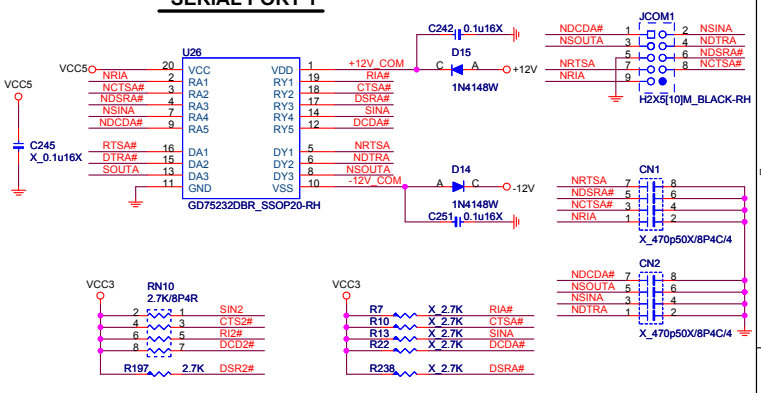
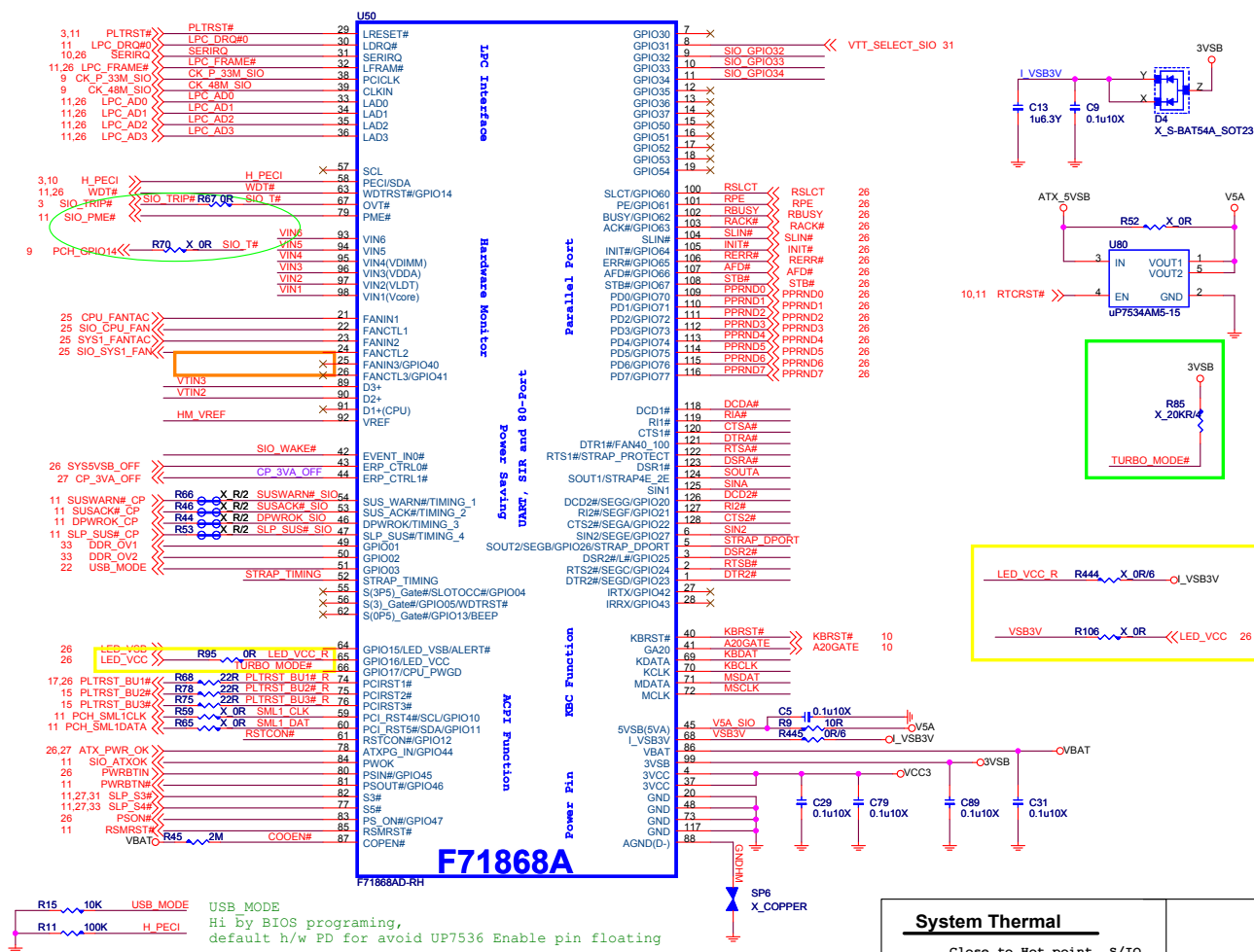
Size
Custom

Document Description
SATA Connector

Date: Friday, May 11, 2012

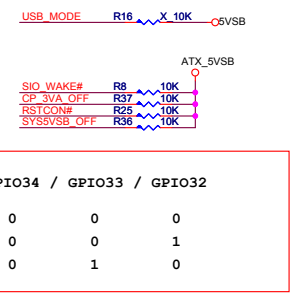
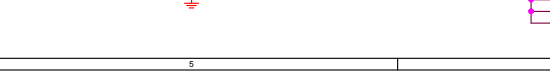
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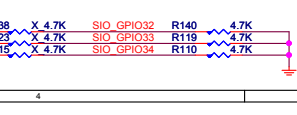


LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

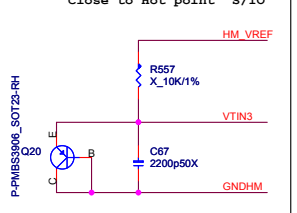
STRAP	Don't STUFF	STUFF
SOUTA#	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courager point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT (SOUT2) Enable 80 Port		Disable 80 Port
RTSA#		



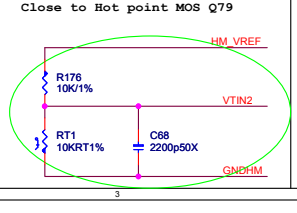
OPT BOM



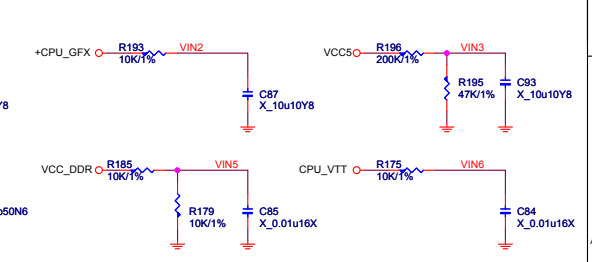
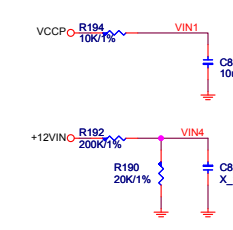
System Thermal



System Thermal

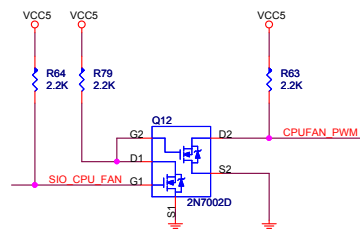


HW Monitor - Voltage

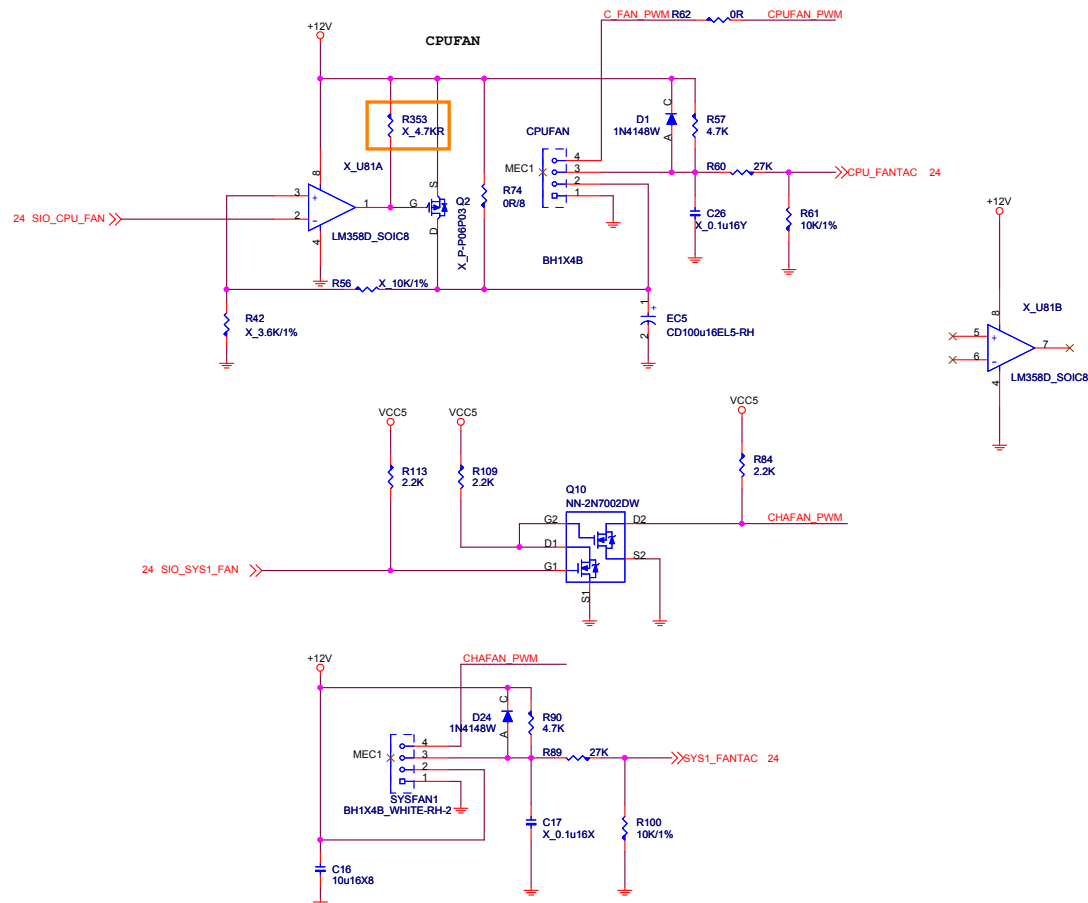
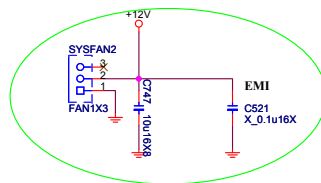


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FAN-COUNTROL CIRCUIT



SYSTEM FAN1



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Size
Custom

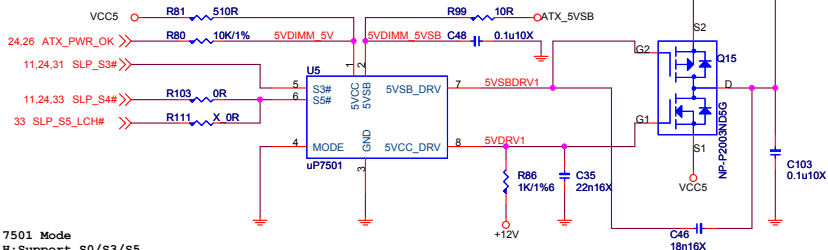
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FAN Control

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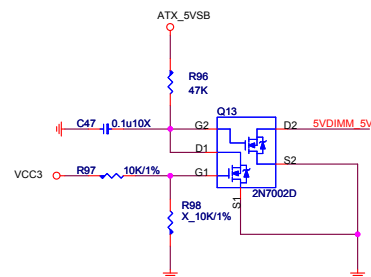
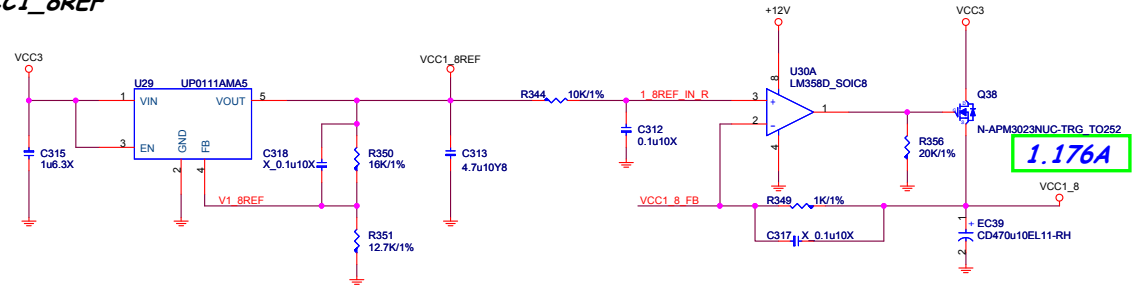
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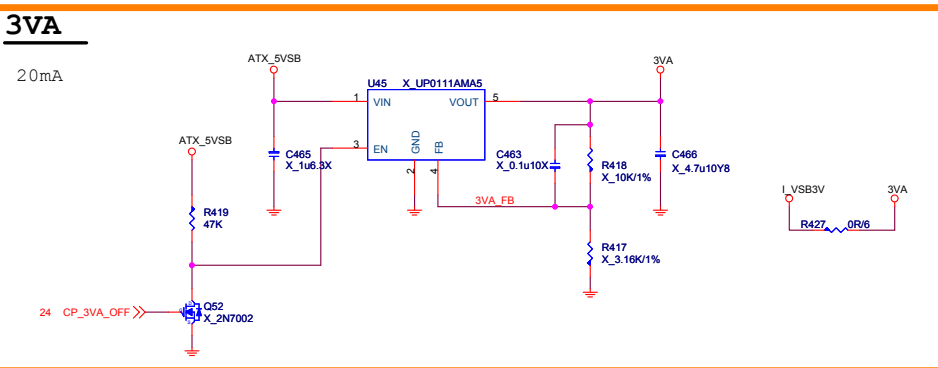
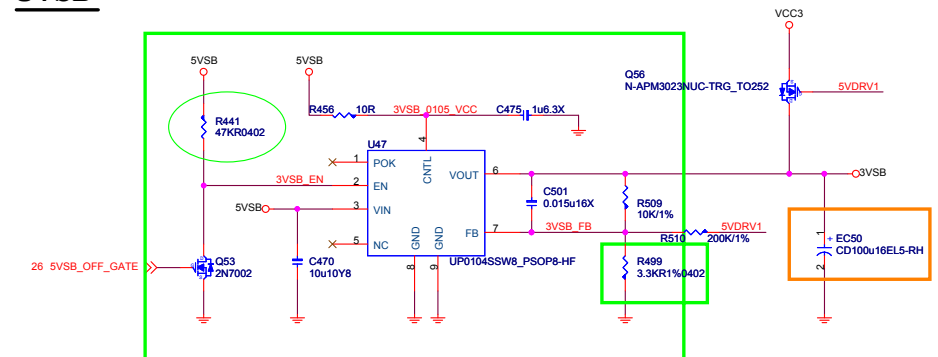

```
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
```



VCC3



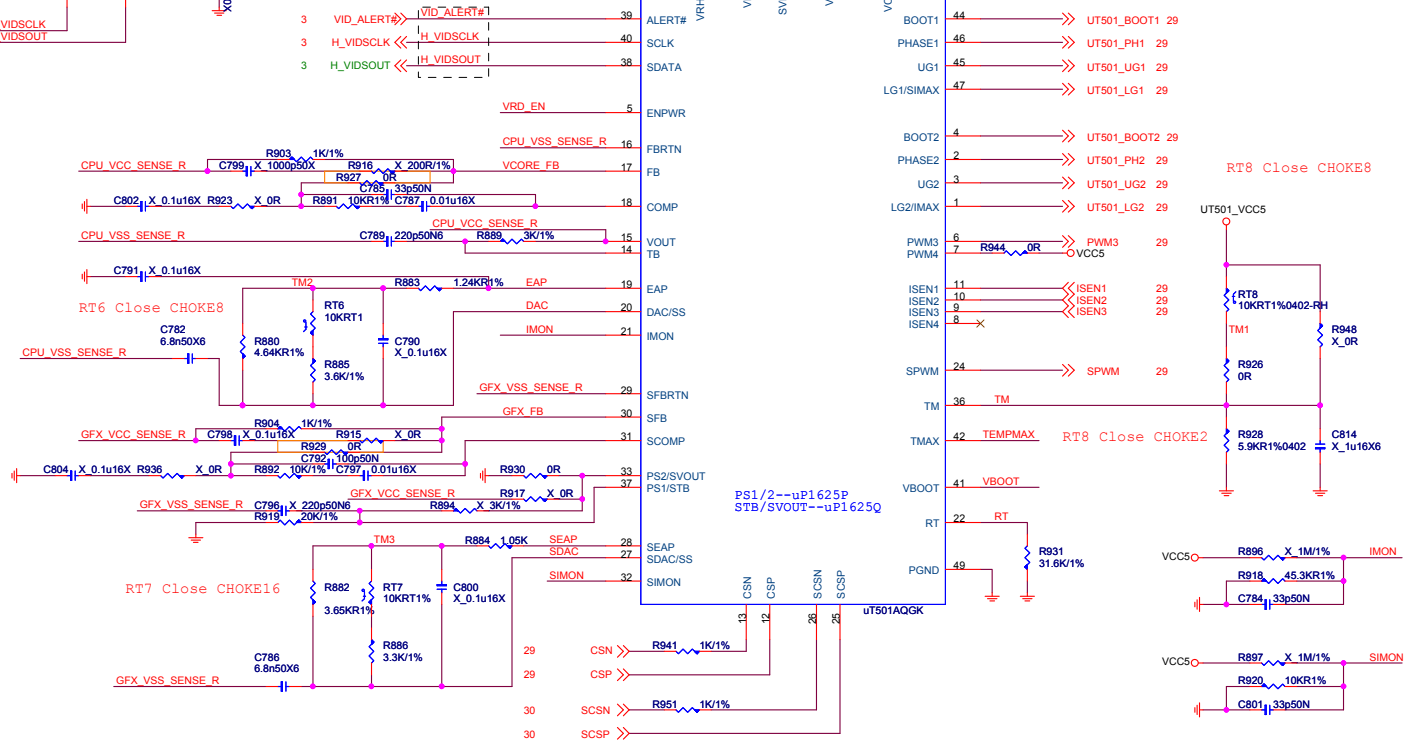
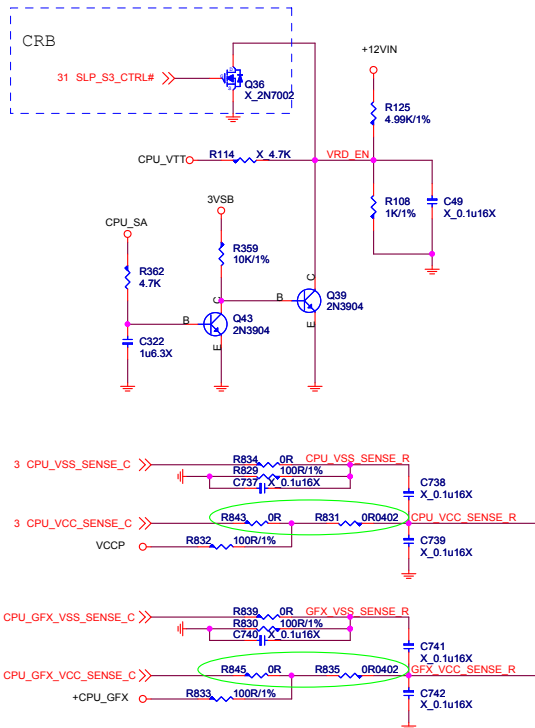
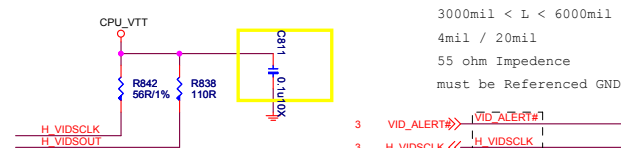
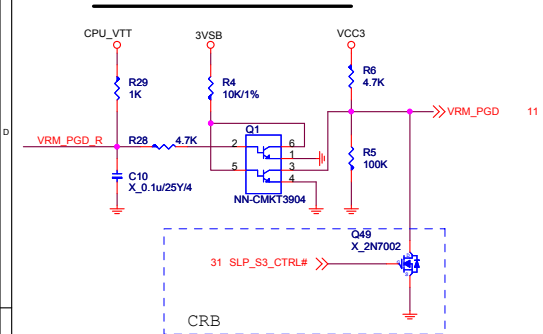
3VA



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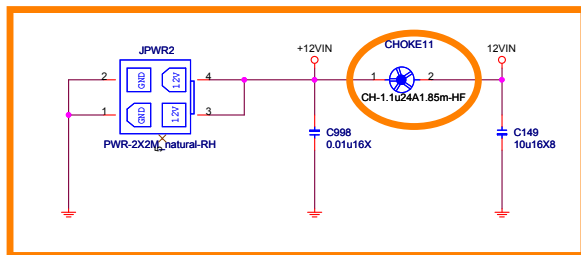
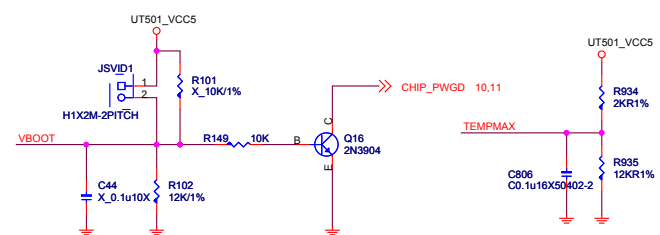
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VRMPWRGD LEVEL SHIFT



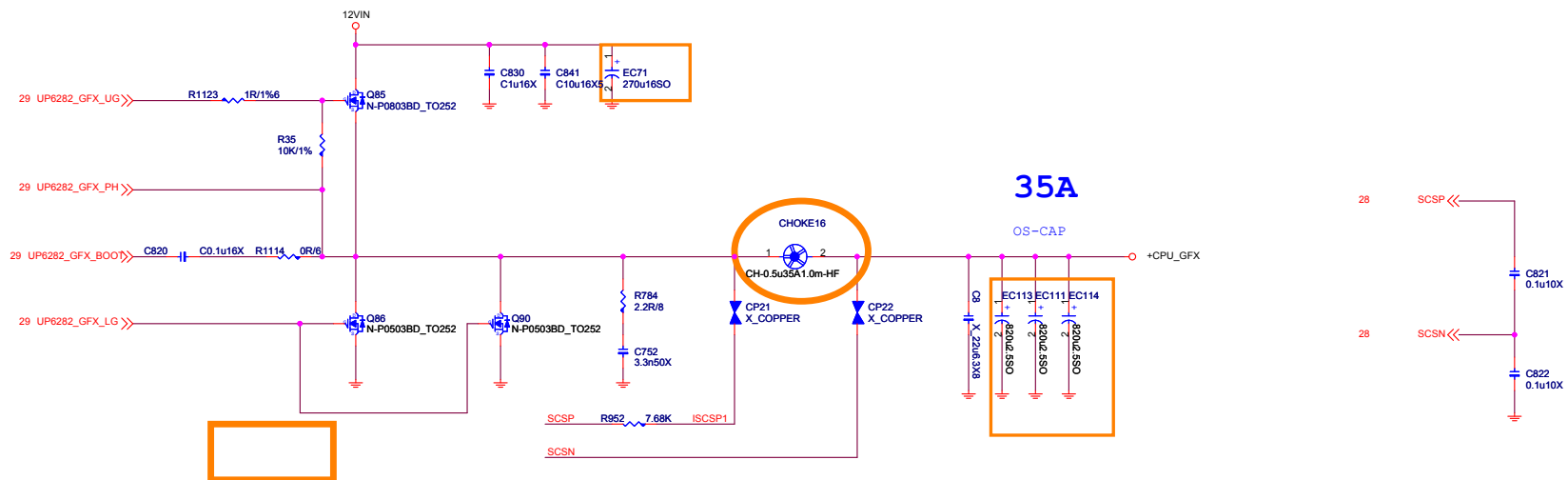
UPI VOLTAGE CONSOLE

	0x20: RH=10K, RL=OPEN					
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%




CPU_GFX:0.25-1.52

35A FOR CPU



CPU_SA:0.925/0.85

SA Core =8.8A

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DDR Power:1.5V

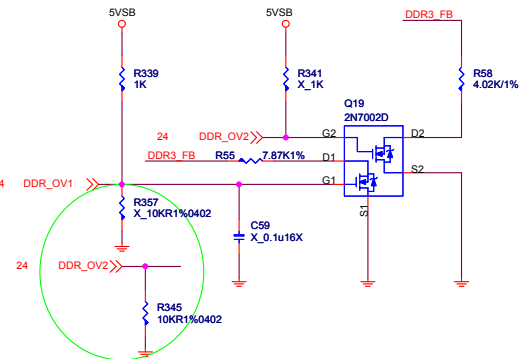
DDR3_1.5V $4.75A+5.5A+0.5A=10.75A$

4.75A FOR CPU

5.5A FOR 2DIMM

0.5A FOR DDR VTT

DDR OV

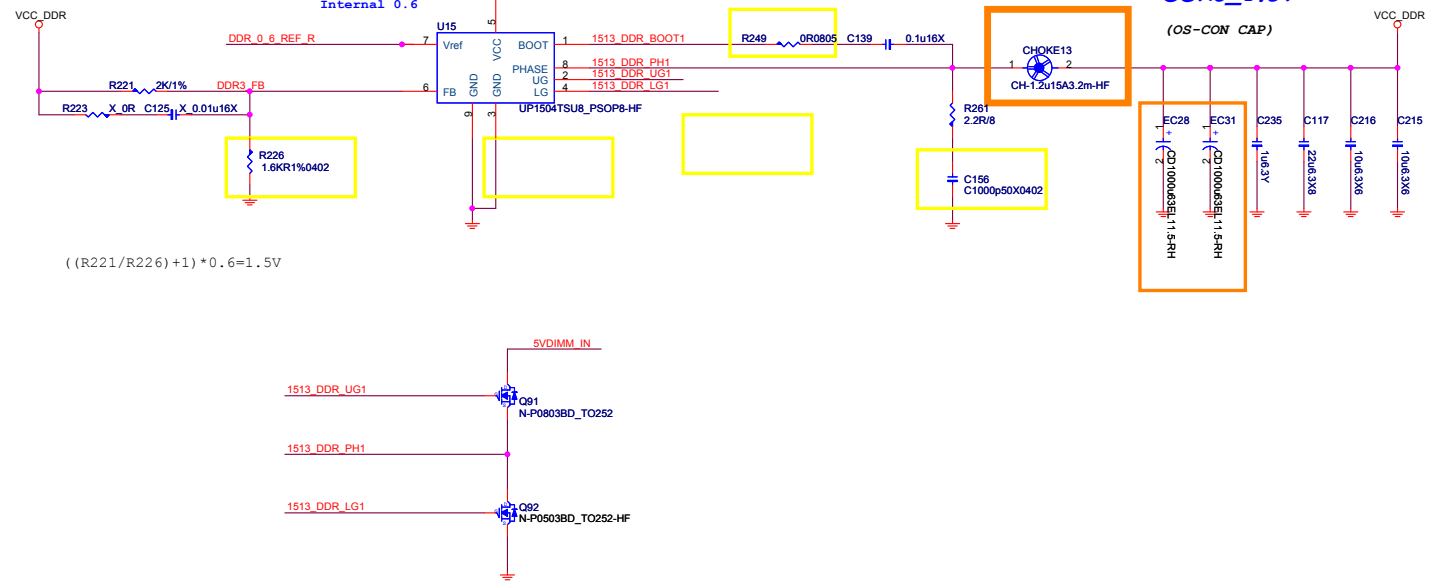


*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01 (S/IO)

DDR_OV2 = GPIO02 (S/IO)

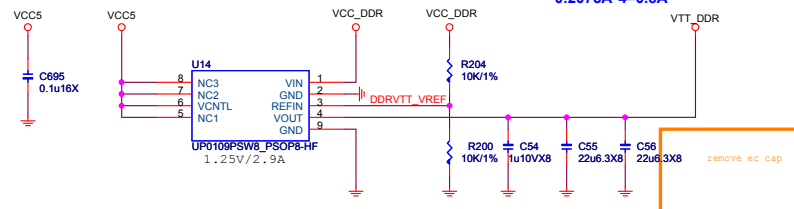


$$((R221/R226)+1) * 0.6 = 1.5V$$

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

$$0.2075A * 4 = 0.8A$$

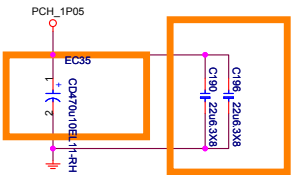


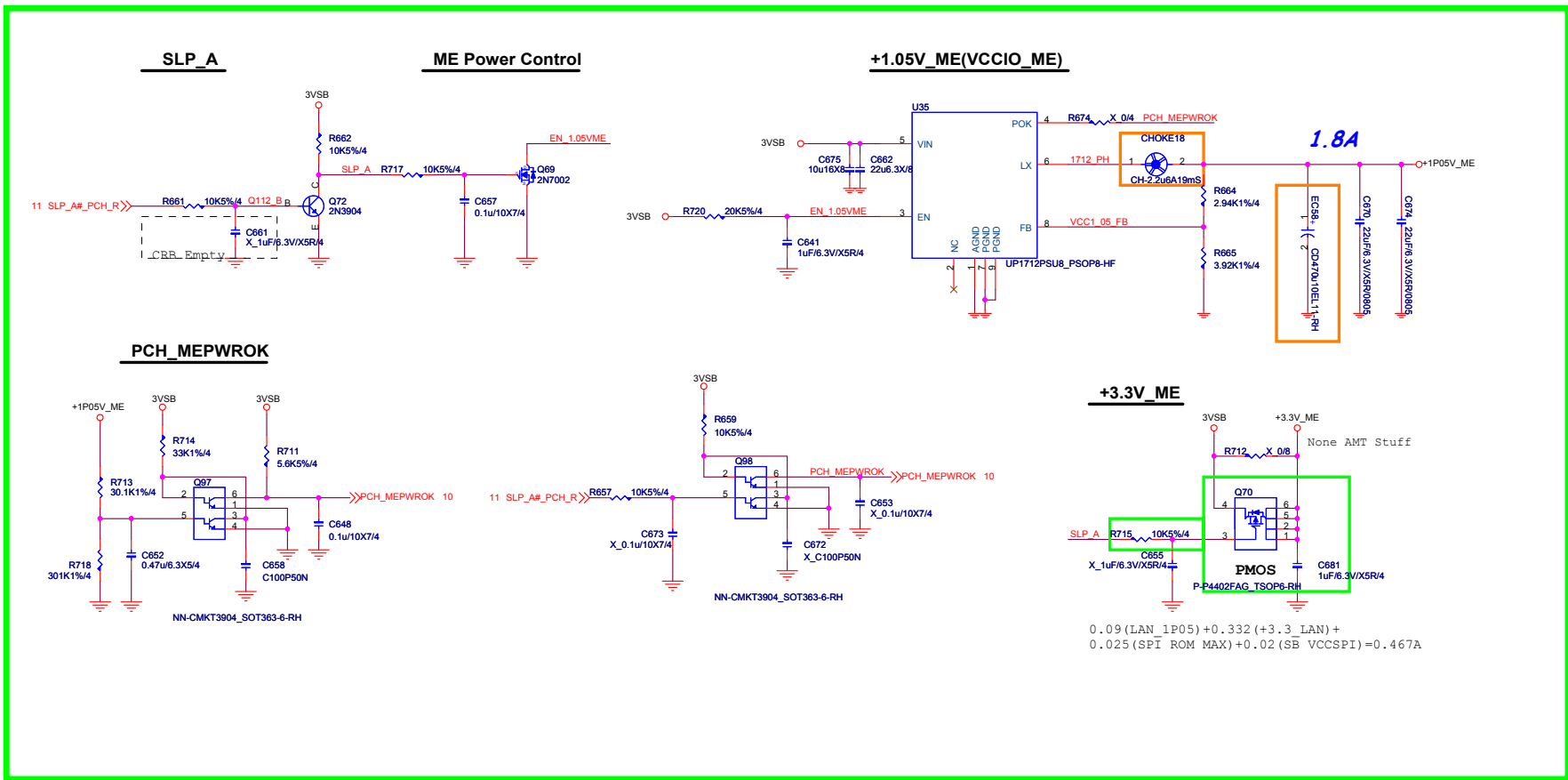
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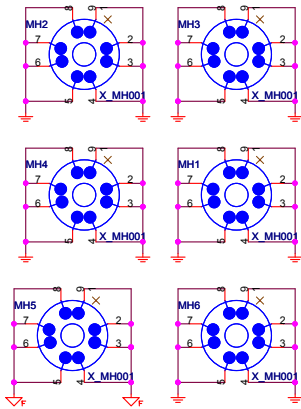
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	DDR Power -UP1513 1-Phase MOS	
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PCH Power:1.05V
PCH Core 6.2A+0.105A+0.5A+0.08A=6.935A
6.2A FOR PCH
0.105A FOR VCCSSC
0.5A FOR VCCPLL
0.08A FOR VCCDMI

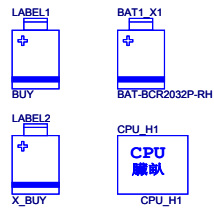
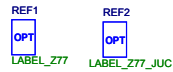
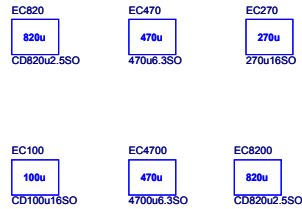




Mounting Holes



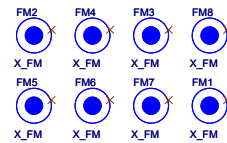
SOLID CAP



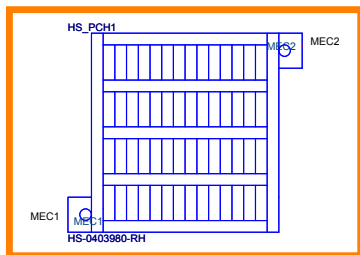
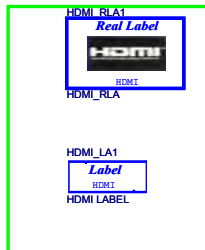
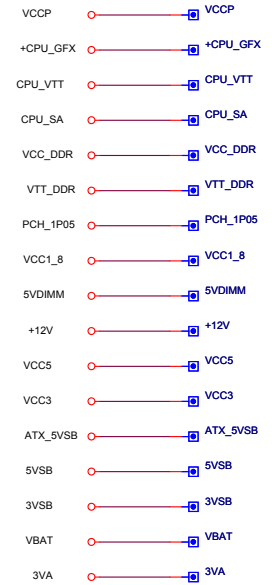
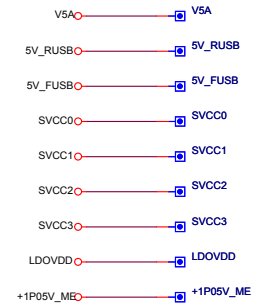
Simulation



Optical Fiducial Marks-120



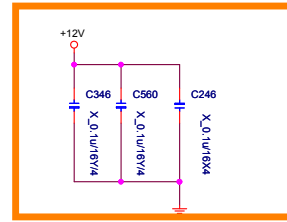
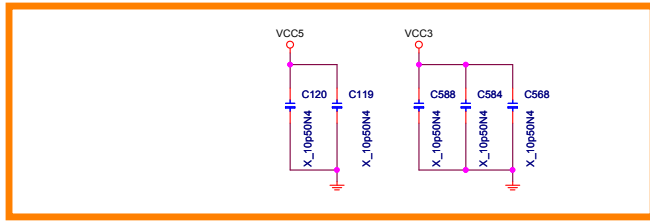
Voltage test point



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EMI:cap. for signal return path

EMI



EMI

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